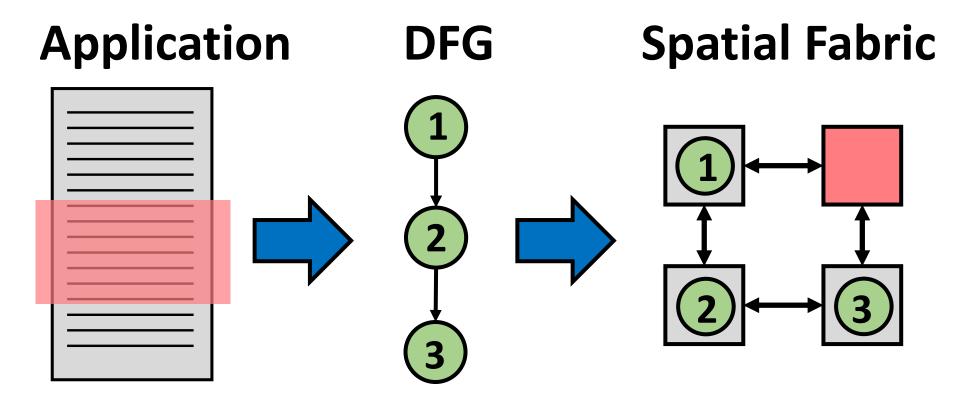
CHAINSAW

Von-Neumman Accelerators To Leaverage Fused Instruction Chains

Amirali Sharifian, **Snehasish Kumar**, Apala Guha, Arrvindh Shriraman

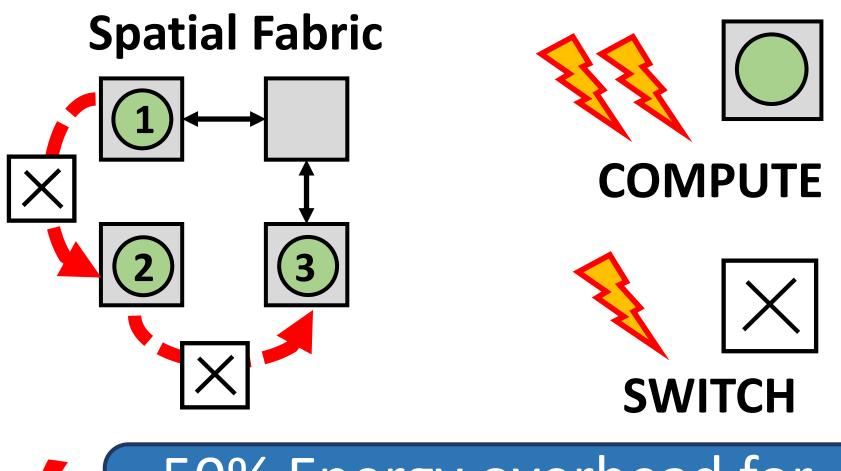


AXC Challenge 1: Idleness



Fabric Size X Dataflow graph size Larger dataflow (possibly more idleness)

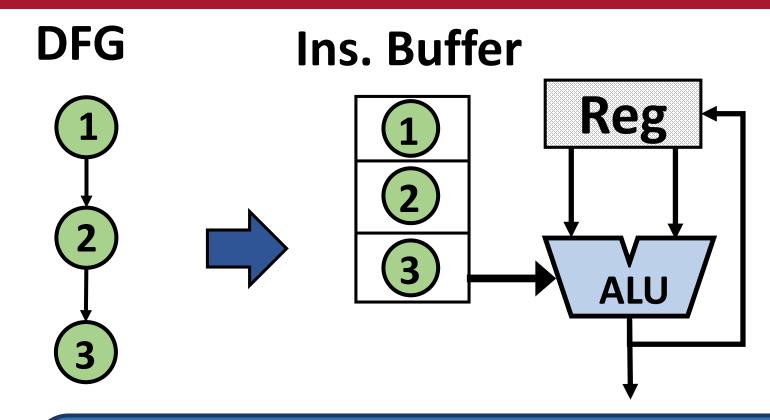
AXC Challenge 2: Data movement





50% Energy overhead for data movement

Von-Neumann Features





Temporal Mapping = Less Idleness Central Register File Fetch and Decode

Our Approach : Fused Instruction Chains

Von-Neumann + Chains **CHAIN DFG** Reg. Compiler 2 2 exposed **Bypass** 3

Temporal Mapping = Less Idleness Bypass = Internalize communication

Our Approach : Fused Instruction Chains

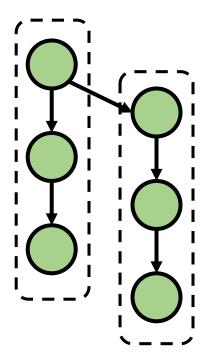
Do chains exist in a DFG? > How to form the chains? > What are the challenges?

Modeling and Evaluation

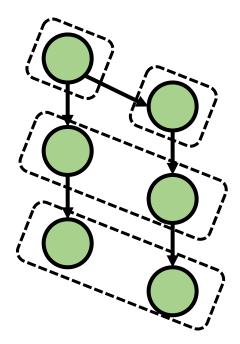
Central Register File

CHAINs vs VLIW

CHAINSAW

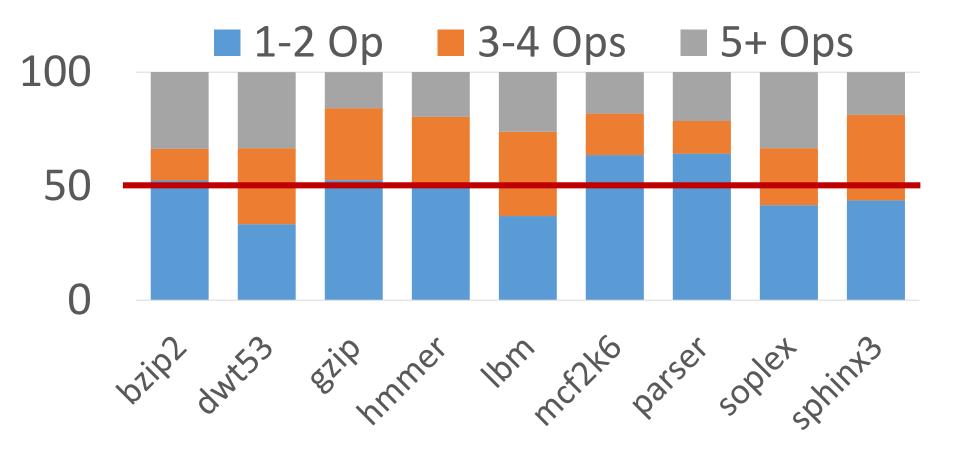






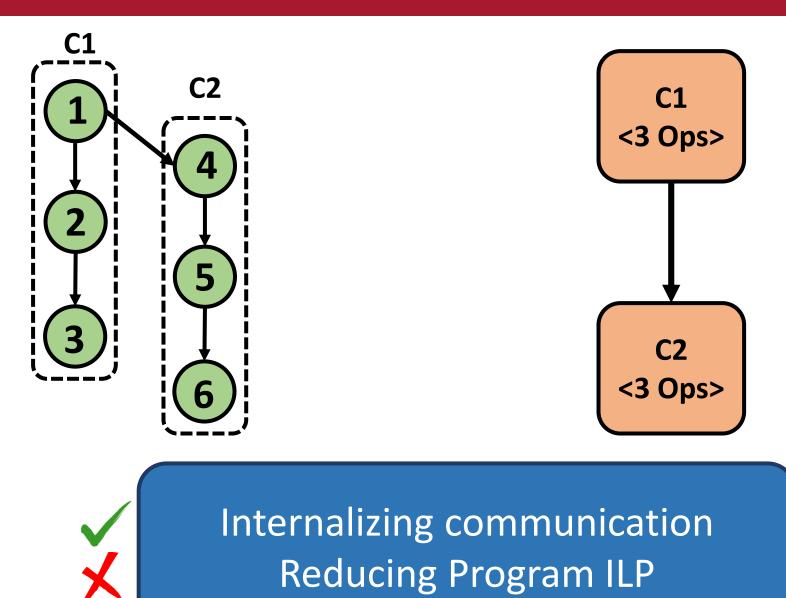
Finding <u>dependent</u> instructions Vertical Fusion Finding <u>independent</u> instructions Horizontal Fusion

Do chains exist in a DFG ?

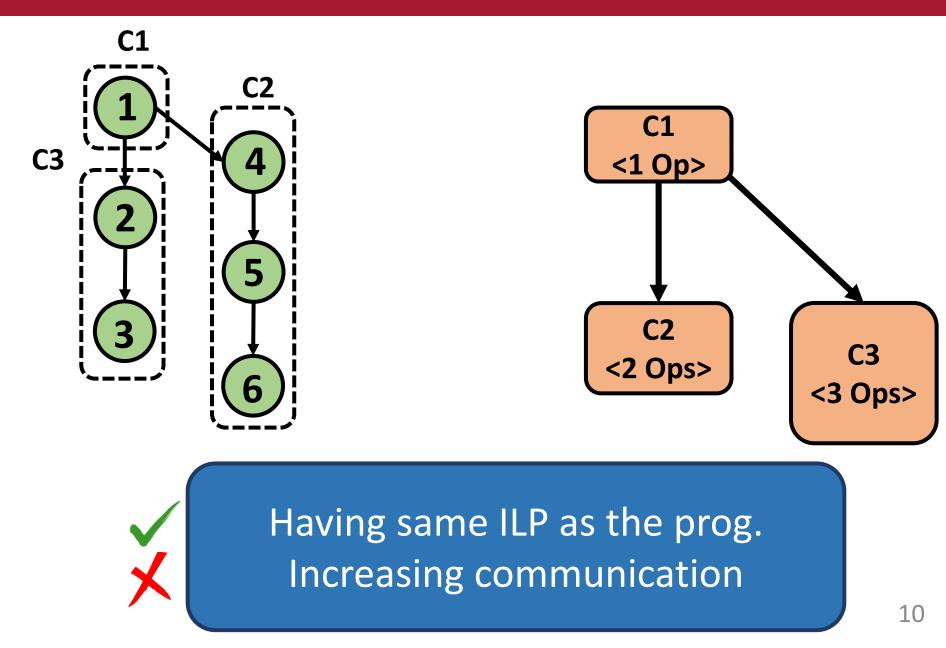


50–80% of DFG part of 3+ op chains

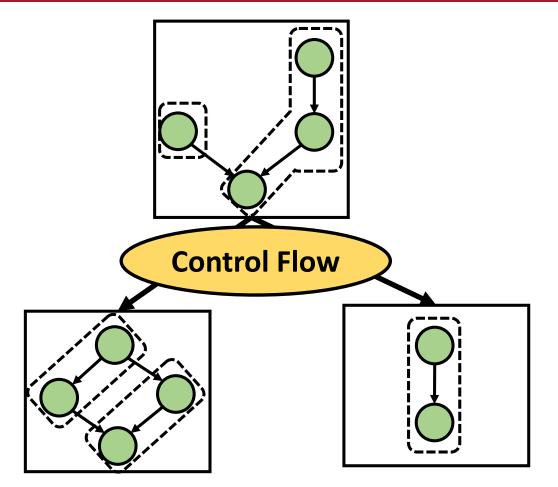
How to form chains? Reduce Comm.



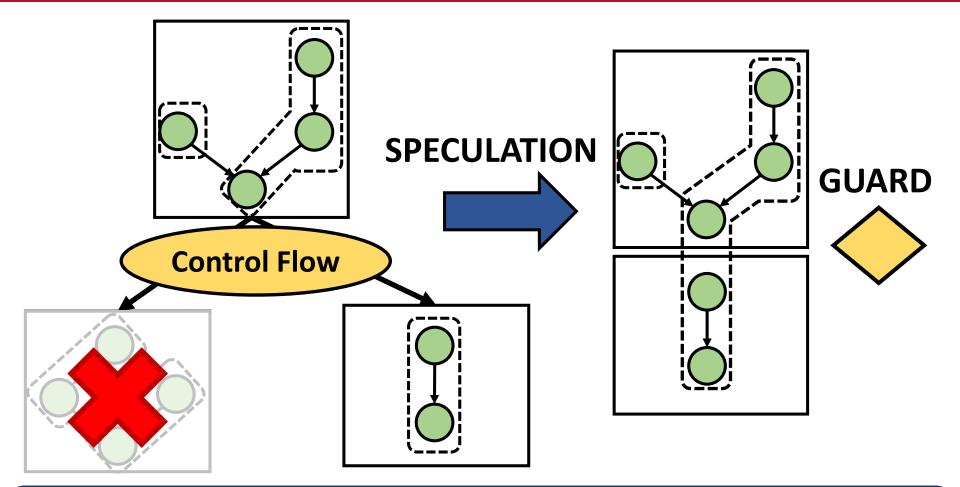
How to form chains? Optimize for ILP



How to extract – *longer* – Chains

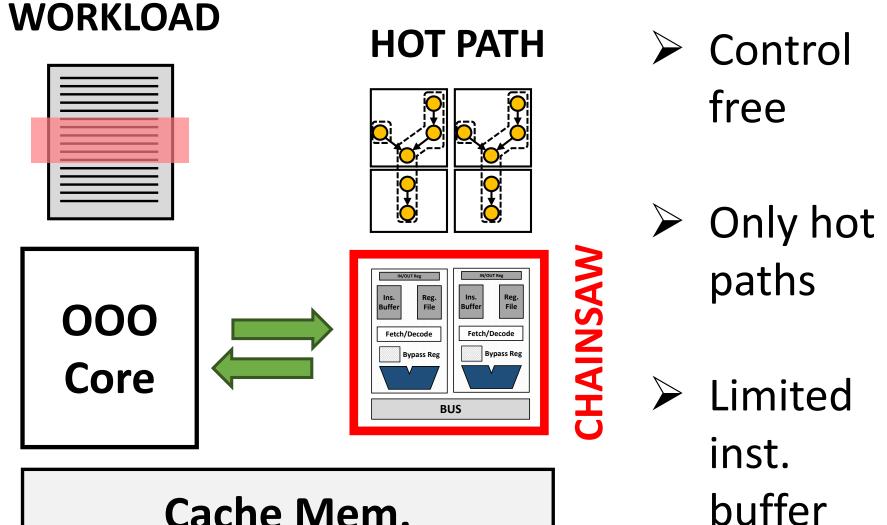


How to extract – *longer* – Chains



Larger Superblocks/Paths \Rightarrow Larger chains

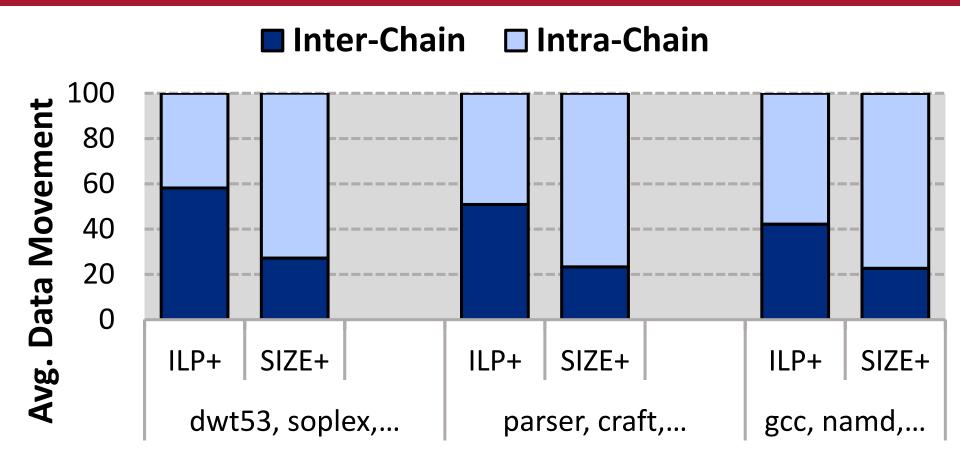
CHAINSAW is an Accelerator



Cache Mem.

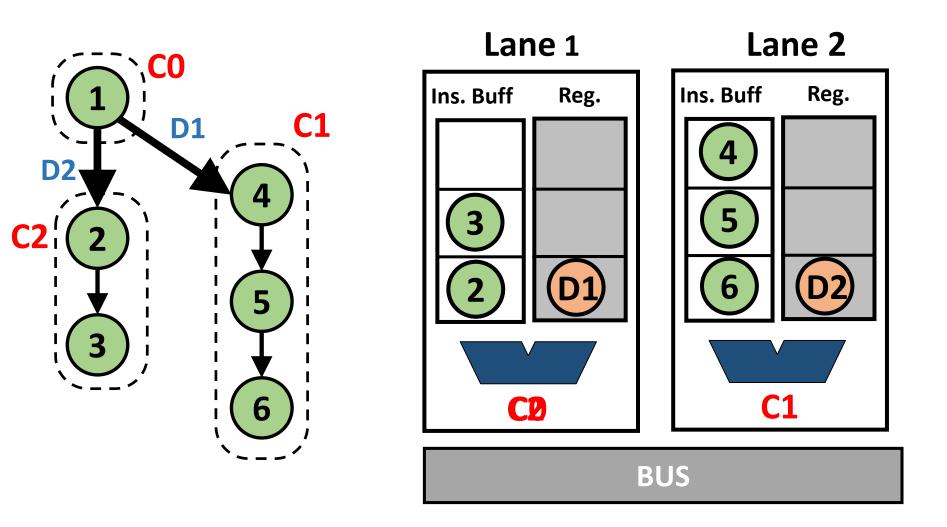
13

How much can we localize?

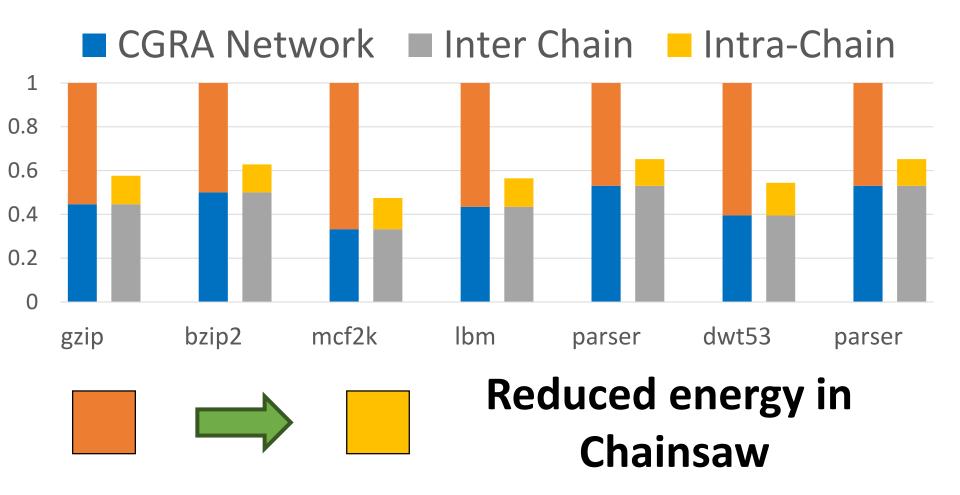


40-60% communication reduction

Multi-Lane CHAINSAW Execution



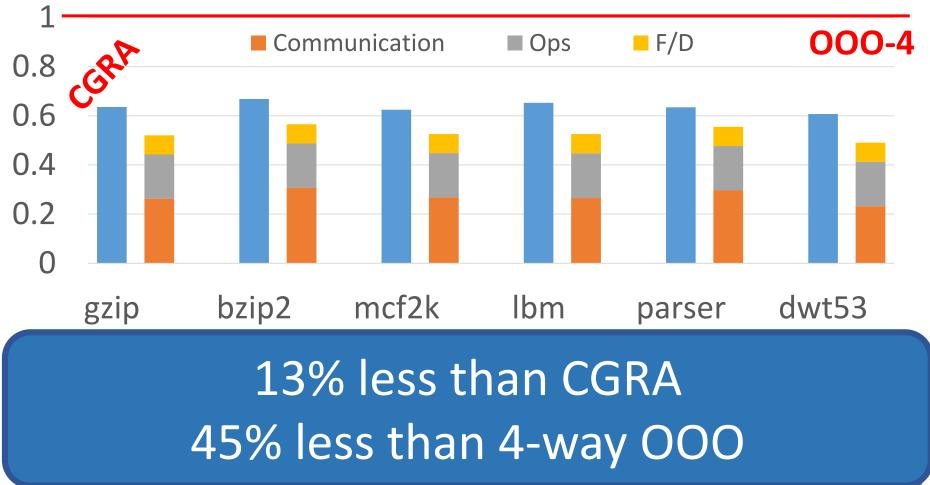
Evaluation – Data movement energy



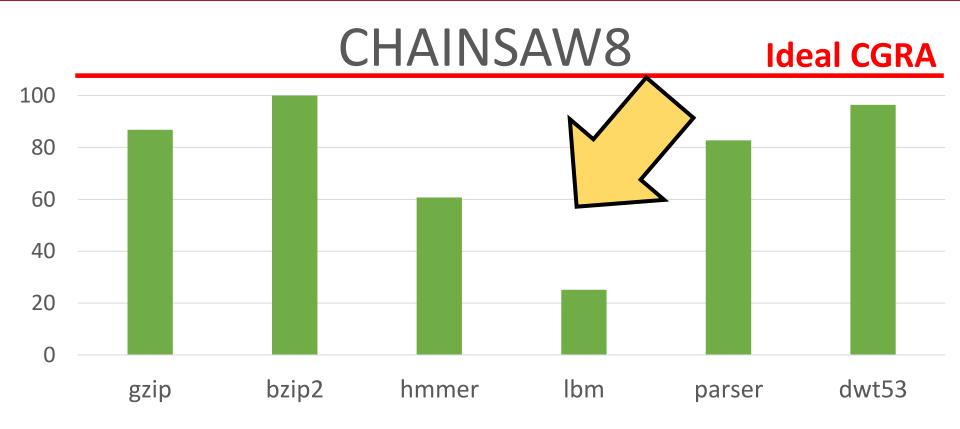
Chainsaw internalizes 50%+ of comm.

Evaluation – Dynamic Energy

- Chainsaw adds Fetch/Decode cost for dynamic energy
- CGRA network overhead dominate Chainsaw F/D cost



Evaluation – Performance

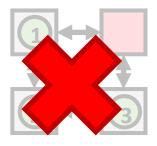


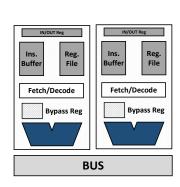
Within 73% of ideal dataflow 20% better than OOO core

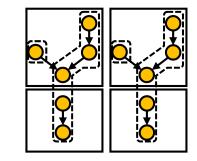
Chainsaw is a Von-Neumman accelerator

- Chains sequentially dependent operations.
- > Chainsaw Accelerator:
 - Target control free regions
 - Reuse functional units
 - Reduce communication energy
 - Lane based architecture

Energy < CGRA Performance \simeq CGRA









Thank you

